AMENDMENTS TO THE SPECIFICATION

The following amendments to the specification are being made for consistency and are supported by the waveforms in Figures 3b, 3c, 4b and 4c and paragraph 25, which describes Figure 19 as a "NOR combinational logic circuit" and paragraph 27, which describes Figure 4a as a "NAND combinational logic circuit."

Please replace the paragraph [00023] with the following amended paragraph:

[00023] However, when voltage ' (N-1) out' 350 is at high level, represented as pulse 354 and voltage '(N+1) out' 360 is at low level, -n-type transistor 310 and the p-type transistor 325 are turned on while n-type transistor 330 and the p-type transistor 320 are turned off. In this case, only the path between terminal 122 and the source terminal of transistor 310 is conducting. Thus, voltage '(N) in' 121 at input terminal 122 is at a level of that of CL_1 145, which is V_{ss}. As voltage '(N) in' 121 is at a low voltage, represented as pulse 126p', it is inverted with regard to input pulse 354. On the other hand, when voltage ' (N-1) out' 350 is at low level and voltage '(N+1) out' 360 is at high level, ~~n-type transistor 330 and~~ the p-type transistor 320 ~~are~~ is turned on while n-type transistors 330 and 310 and p-type transistor 325 are turned off. In this case, the drain of transistor 330 is forced to a high level by its gate/drain capacitance and only the path between input terminal 122 of shift register stage 120 and the drain ~~source~~ terminal of transistor 330 is conducting. Thus, the voltage '(N) in' 121 at input terminal 122 remains substantially at a high level, i.e., V_{dd}. The pulsed signal '(N+1) out' is blocked away

from triggering shift register stage (N) by the invented bi-directional circuit under forward shifting operation.

Please replace the paragraph [00033] with the following amended paragraph:

[00033] Further, when voltage '(N+1)*out' 460 is at high level and voltage '(N-1)*out' 450 transitions from a high level to a ~~is at~~ low level, represented as inverse pulse 454, n-type transistor 425 ~~and p-type transistor 410 are~~ is turned on while the n-type transistor 420 and the p-type transistors 430 and 410 are turned off. In this case, the gate to drain capacitance of transistor 410 forces the drain of transistor 410 to a low state when (N-1)* transitions from a high level to a low level. With the drain of transistor 410 at a low state, the path between input terminal 122 of shift register stage 120 and the drain ~~source~~ terminal of transistor 410 is conducting so that the voltage '(N) in' 121 is substantially at a level of that of ~~CL_1 145, which is~~ V_{ss}. In this case, voltage (N) in 121 remains at its normally low level state.